94, respectively. Likewise, the outputs of inverters 102, 104, and 106 are connected to the sources of transistors 88, 92, and 96, respectively. The second plate of capacitor 56 is connected to ground. The output of buffer amplifier 98 is the output of the circuit. The programmable delay control circuit 80 can be constructed using many common digital circuits including input/output device, RAM memory, ROM memory, EPROM, EEPROM, and the like.

In operation, this embodiment operates in an analogous manner to the previous embodiment, but with the added feature that capacitor 56 can now be charged or discharged by one or more pairs of current mirrors. Transistors 48 and 50 are the input transistors; transistors 42 and 46 are the bias transistors; transistors 82, 86, 90, and 94 are the constant-current source transistors; and transistors 84, 88, 92, and 96 are the constant-current drains, for this embodiment.

More specifically, an input signal enters the circuit through the gate of transistor 48 which turns on transistor 42. Since the gate of transistor 42 is connected to the gates of transistors 82, 86, 90, and 94, transistor 42 provides the bias voltage for transistors 82, 86, 90, and 94 such that the current flow in the respective transistor is proportional (mirrored) to the current through transistor 42. However, transistors 82, 86, 90, and 94 will only be turned on if programmable delay control circuit 80 has enabled one of those transistors by providing the source of the respective transistor with a positive voltage. Therefore, the rate of delay or the rate of charging capacitor 56 is controlled by the programmable delay control circuit 80 and the relative ratios of transistors 42 to transistors 82, 86, 90, and 94. Inversely, when the input signal goes low, transistor 50 turns on bias transistor 46 which thereby provides the bias voltage to turn on transistors 84, 88, 92, and 96 to remove the charge from capacitor 56. Again, transistors 84, 88, 92, and 96 will not drain any current from capacitor 56 unless the transistors have been enabled by programmable delay control circuit 80 providing a sufficiently low voltage to the respective transistors drain. In this disclosure, it is assumed that the enable signals from the programmable delay control signal are digital in nature with sufficient current drive to drive the MOSFET transistors.

It will be clear to persons skilled in the art that additional transistor pairs can be added to the circuit to increase the range of programmability. Four transistor pairs are disclosed for illustrative purposes and could easily be modified to less pairs or more pairs by persons skilled in the art. Additionally, persons skilled in the art can vary the ratio of the current mirrors to further increase the range of programmability. By adjusting the current mirror ratios and/or increasing the number of transistor pairs persons skilled in the art can easily design a programmable delay which meets a given design criteria for versatility as well as flexibility.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

We claim:

1. A delay circuit comprising:

a plurality of current mirror current sources, with each current mirror current source having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a plurality of current mirror current drains, with each current mirror current drain having an enable input,

having an input for receiving the input signal, and having a constant drain output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each signal connected to a current mirror current source and current mirror current drain such that the programmable delay control circuit selectively enables a pair of current mirror current source and drain;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current sources and to the constant drain outputs of the plurality of current drains, the second plate connected to a voltage reference, with each current mirror current source having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor and with, each current mirror current drain having a current path between the corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor

wherein a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor, and

wherein a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

2. The delay circuit of claim 1 wherein the programmable delay control circuit comprises a digital circuit.

3. The delay circuit of claim 2 wherein the digital circuit comprises programmable memory circuit.

4. The delay circuit of claim 3 wherein the programmable memory circuit comprises a programmable read only memory.

5. The delay circuit of claim 4 wherein the programmable read only memory comprises a EEPROM.

6. The delay circuit of claim 3 wherein the programmable memory circuit comprises a FLASH memory.

7. A delay circuit comprising:

a first input transistor having a control element for receiving an input signal, and having a current path with a first end connected to a voltage source and a second end;

a second input transistor having a control element for receiving the input signal, and having a current path with a first end and a second end connected to a voltage reference;

a first bias transistor having a current path with a first end connected to the voltage source, having second end, and having a control element, wherein the second end is connected to the control element and to the second end of the current path of the first input transistor;

a resistor having a first end connected to the second end of said first bias transistor and having a second end;

a second bias transistor having a current path from the second end of said resistor to the voltage reference, and having a control element connected to the second end of said resistor and to the first end of the current path of said second input transistor;

a capacitor having a first plate and having a second plate connected to the voltage reference;

an output stage having an input connected to the first plate of said capacitor and having an output;

a programmable delay control circuit having a plurality of enable outputs;

a plurality of constant-current sources, each constant current source of the plurality of constant-current sources having a current path between a corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said first bias transistor such that the current flowing in the first bias transistor is proportionately mirrored in the current path of each constant-current source of the plurality of constant-current sources, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current source; and

a plurality of constant-current drains, each constant current drain of the plurality of constant-current drains having a current path between the corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said second bias transistor such that the current flowing in the second bias transistor is proportionately mirrored in the current path of each constant-current drain of the plurality of constant-current drains, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current drain.

8. The delay circuit of claim **7** wherein said programmable delay control circuit comprises a digital circuit.

9. The delay circuit of claim **8** wherein the digital circuit comprises programmable memory circuit.

10. The delay circuit of claim **9** wherein the programmable memory circuit comprises a programmable read only memory.

11. The delay circuit of claim **10** wherein the programmable read only memory comprises a EEPROM.

12. The delay circuit of claim **9** wherein the programmable memory circuit comprises a FLASH memory.

13. A delay circuit comprising:

a plurality of current mirror current elements, with each current mirror current element having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each enable signal connected to the plurality of current mirror current elements so as to selectively enable a current mirror current element of the plurality of current mirror current elements;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current elements, the second plate connected to a voltage reference, with each current mirror current element having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor,

wherein a delay on an active edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current elements to change an overall current provided by the plurality of current mirror current elements to the first plate of the capacitor.

14. The delay circuit of claim 13, wherein the active edge of the input signal is a rising edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current sources, and a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor.

15. The delay circuit of claim 13, wherein the active edge of the input signal is a falling edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current drains, and a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

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